

<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANTS PTO-1449</b>	Attorney Docket No. <b>2885/56</b>	Serial No. <b>10/009,649</b>
	Applicant(s) <b>Martin Vorbach et al.</b>	
	Filing Date <b>May 29, 2002</b>	Group Art Unit <b>2192</b>

**U.S. PATENT DOCUMENTS**

EXAMINER'S INITIALS	PATENT/ PUBLICATION NUMBER	PATENT/PUBLICATION DATE	NAME	CLASS	SUBCLASS	FILING DATE
	4,623,997	November 18, 1986	Tulpule			
	5,212,777	May 18, 1993	Gove et al.			
	5,572,710	November 5, 1996	Asano et al.			
	5,606,698	February 25, 1997	Powell			
	5,659,785	August 19, 1997	Pechanek et al.			
	5,696,791	December 9, 1997	Yeung			
	5,804,986	September 8, 1998	Jones			
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	6,434,672	August 13, 2002	Gaither			
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	6,553,479	April 22, 2003	Mirsky et al.			
	6,606,704	August 12, 2003	Adiletta et al.			
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	7,382,156	June 3, 2008	Pani et al.			
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**FOREIGN PATENT DOCUMENTS**

EXAMINER'S INITIALS	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION	
						YES	NO
	3-961028	August 15, 2007	Japan			Abstract	
	2001-510650	July 31, 2001	Japan			Abstract only	
	2002-0033457	January 31, 2002	Japan			Abstract	

**OTHER DOCUMENTS**

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	Altera, "2. TriMatrix Embedded Memory Blocks in Stratix & Stratix GX Devices," Altera Corporation, July 2005, 28 pages.
	Altera, "APEX II Programmable Logic Device Family," Altera Corporation Data Sheet, August 2002, Ver. 3.0, 99 pages.
	Becker, J., "A Partitioning Compiler for Computers with Xputer-based Accelerators," 1997, Kaiserslautern University, 326 pp.
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	"BlueGene/L: the next generation of scalable supercomputer," Kissel et al., Lawrence Livermore National Laboratory, Livermore, California, November 18, 2002, 29 pages.
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	BlueGene/L, "An Overview of the BlueGene/L Supercomputer," The BlueGene/L Team, IBM and Lawrence Livermore National Laboratory, 2002 IEEE. pp. 1-22.
	Epstein, Dave, "IBM Extends DSP Performance with Mfxt," Microprocessor Report, Vol. 9, No. 16 (MicroDesign Resources), December 4, 1995, pp. 1-4 [XL0029013].

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EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
	Galanis, M.D. et al., "Accelerating Applications by Mapping Critical Kernels on Coarse-Grain Reconfigurable Hardware in Hybrid Systems," Proceedings of the 13 <sup>th</sup> Annual IEEE Symposium on Field-Programmable Custom Computing Machines, 2005, 2 pages.
	Guo, Z. et al., "A Compiler Intermediate Representation for Reconfigurable Fabrics," University of California, Riverside, Dept. of Electrical Engineering, IEEE 2006, 4 pages.
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	Hartenstein et al., "Parallelizing Compilation for a Novel Data-Parallel Architecture," 1995, PCAT-94, Parallel Computing: Technology and Practice, 13 pp.
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	Jo, Manhwee et al., "Implementation of Floating-Point Operations for 3D Graphics on a Coarse-Grained Reconfigurable Architecture," Design Automation Laboratory, School of EE/CS, Seoul National University, Korea, IEEE 2007, pp. 127-130.
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EXAMINER	DATE CONSIDERED
EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	